



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,011	07/03/2002	Gilbert Wolrich	10559-312US1	5760

20985 7590 04/04/2005

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER

TREAT, WILLIAM M

ART UNIT	PAPER NUMBER
----------	--------------

2183

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/070,011

Applicant(s)

WOLRICH ET AL.

Examiner

William M. Treat

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2183

1. Claims 1-36 are presented for examination.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Applicants claim in claim 1 and its dependent claims 2-29: "one of the instructions causing the ALU to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting." On pages 9 and 10 of applicants' specification, they state: "The micro engine 22f includes an execution box (EBOX) data path 76 that includes an arithmetic logic unit (ALU) 76a and general-purpose register set 76b. The ALU 76a performs arithmetic and logical functions as well as shift functions." Further down on page 10, applicants state: "Referring to FIG. 4, the micro engine data path maintains a 5-stage micro-pipeline 82. This pipeline includes lookup of microinstruction words 82a, formation of the register file addresses 82b, read of operands from register file 82c, ALU shift or compare operations 82d, and write-back of results to registers 82e." These few sentences represent the sum of the ALU duties discussed in applicants' original disclosure, as best the examiner has been able to determine. There is no discussion of an ALU issuing "a memory reference to an address in a memory shared among threads". Applicants do state on page 3 of

Art Unit: 2183

their specification that “The micro engines 22a-22f can execute memory reference instructions to either the SDRAM controller 26a or SRAM controller 16b.” Also, on page 3 applicants state:

“The SRAM controller 26b controls arbitration for the SRAM bus, accesses the SRAM 16b, fetches the data from the SRAM 16b, and returns data to a requesting micro engine 22a-22f.

During an SRAM access, if the micro engine, e.g., micro engine 22a had only a single thread that could operate, that micro engine would be dormant until data was returned from the SRAM 16b.

By employing hardware context swapping within each of the micro engines 22a-22f the hardware context swapping enables other contexts with unique program counters to execute in that same micro engine. Thus, another thread, e.g., Thread_1 can function while the first thread, i.e., Thread_0, is awaiting the read data to return.” There is nothing in applicants’ original disclosure stating the ALU issues a memory reference for the micro engines merely that “The micro engines 22a-22f can execute memory reference instructions to either the SDRAM controller 26a or SRAM controller 16b.” In fact Fig. 4 makes it appear that a read of (i.e., memory reference to) shared memory would not be an ALU function. Applicants’ original disclosure is silent as to the duties of the ALU in any memory reference.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. See paragraph 4, *supra*, for a relevant explanation of the deficiency.

Art Unit: 2183

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-23, 26, and 30-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Agarwal et al. (APRIL: A Processor Architecture for Multiprocessing).

10. The reasons set forth in the examiner's previous actions for rejecting claims 1-23, 26, and 30-36, as being anticipated by Agarwal, continue and are hereby incorporated by reference.

11. Applicant's arguments filed 3/18/2005 have been fully considered but they are not persuasive.

12. Applicants have argued on behalf of independent claims 1 and 30 and their dependent claims that Agarwal does not teach "causing the ALU to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting" or similar language, and "Applicants' invention concerns multiple threads executing in multiple microengines, while Agarwal discloses merely a single SPARC-based processor that supports four hardware contexts." As noted in paragraph 4, *supra*, the examiner does not think even applicants disclosed what is claimed. However, if applicants are merely claiming a microengine/microprocessor can issue such a memory reference for a thread while some other thread on some other microprocessor is inactive, Agarwal certainly taught that (pp. 104-106, Sections 2 and 3 in their entirety). Agarwal states: "APRIL is the processing element of ALEWIFE, a large-scale multiprocessor being designed a MIT. ALEWIFE is a cache-coherent machine with distributed, globally-shared memory." (Section 2, first sentence) He also states:

Art Unit: 2183

“As shown in Figure 1, each ALEWIFE node consists of a processing element, floating-point unit, cache, main memory, cache/directory controller, and a network routing switch.” And, “On exception conditions such as cache misses and failed synchronization attempts, the controller can choose to trap the processor or make the processor wait.” (Section 2.1) At the top of page 107, Agarwal further states: “APRIL continues executing a single thread until a memory operation involving a remote request (or an unsuccessful synchronization attempt) is encountered.” Note that Agarwal describes a multiple node processor with each node containing a microprocessor/microengine based on Sun Microsystem’s SPARC processor, with each SPARC processor capable of supporting four hardware contexts/threads, and with threads capable of making memory requests to the distributed, globally-shared memory in Sections 2, 2.1, 2.2, 3, 3.1, 3.2, 3.3, and 3.4. In Section 4 under the title “Memory Instructions” Agarwal describes the memory instructions used by his microprocessor/microengine that will result in the cache/directory controller of his microprocessor/microengine continuing to execute the memory access to the shared memory while the relevant context has been swapped out and is waiting. Applicants’ language of independent claim 1, which is supported by their original disclosure, fails to distinguish over the prior art of record as does the language of independent claim 30.

13. Also, while applicants have not argued the point, the examiner considers the newly-claimed elements of applicants’ microprocessors/microengines to be inherent in the Agarawal system based on Sun Microsystems 1988 version of their SPARC processor (p. 105, lines 7-8 and reference 23 under References on p. 114).

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2183

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claims 24-25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarawal et al. (APRIL: A Processor Architecture for Multiprocessing).

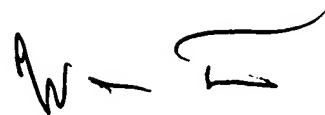
17. The reasons set forth in the examiner's previous actions for rejecting claims 24-25 and 27-29 continue and are hereby incorporated by reference.

18. Applicants have merely argued that the language of independent claims 1 and 30 allow claims 24-25 and 27-29 to distinguish over the art. As to the examiner's response, see paragraphs 4 and 12, *supra*.

19. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

Art Unit: 2183

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**WILLIAM M. TREAT
PRIMARY EXAMINER**